Attorney's Docket No.: 10559-395001/P10260 - ADI APD1811-1-US

REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

Claims 1, 2, 4-8, 17, and 18 stand rejected under 35 USC § 102(b), based on Garibay, Jr. et al. and claims 3, 20, and 19 stand rejected under 35 USC § 103 as being unpatentable over Garibay. These rejections are respectfully traversed.

Claim 1 defines storing a plurality of instructions in at least two prefetch buffers, wherein an instruction and the associated exception word may be spread across more than one prefetch buffer. Moreover, claim 1 defines obtaining each instruction and the associated exception word from the at least two prefetch buffers.

Claim 17 defines a prefetch unit having at least two prefetch buffers. It also clarifies that the control unit may fetch at least two data blocks associated with a single instruction and store exception status information and the data blocks in the prefetch unit in at least two of the prefetch buffers.

As stated in the office action, Garibay does not disclose, inter alia, storing of instructions / status words in at least two prefetch buffers. In addition, Garibay does not disclose the buffering and the subsequent obtaining of the instructions and the associated status words in at least two prefetch buffers. Moreover, Garibay does not disclose that an instruction and the associated exception word may be spread across more than one prefetch buffer.

Therefore, the claims are novel.

Furthermore, there is no suggestion within Garibay for a skilled artisan to provide the method and system as claimed. Garibay does not contemplate using at least two prefetch

buffers, nor does it contemplate buffering an instruction and the associated status word in at least two prefetch buffers. This is much more than merely using multiple buffers to temporarily store data, since it also requires aligning the instructions using the exception word.

The subject matter of claims 1 and 17 ensure that the correct exception word along with the correct instructions is obtained from the correct prefetch buffer or buffers and properly aligned. Such an arrangement may reduce or avoid pipeline bubbles and stalls and the like that can occur if the alignment unit does not properly associate the information in the instructions with the exception information. Garibay does not teach or suggest these features.

Accordingly, all of the claims are non-obvious over the cited art and are allowable.

It is believed that all of the pending claims have been addressed in this paper. However, failure to address a specific rejection, issue or comment, does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above are not intended to be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

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Applicant asks that all claims be allowed. Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 1/4/05

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